II. AMENDMENTS TO THE SPECIFICATIONS:

Please replace paragraph 27 of the specification with the following amended paragraph:

[0027] FIGS. 8-16 show continuing steps of well known SIGe technology that ultimately result in the final high performance NPN and PNP transistors. These steps are outlined in ~~U.S. Patent No. 5,111,271~~ Comfort *et al.* (U.S. Patent No. 5,117,271), hereby incorporated by reference. It should be recognized that theses steps may vary somewhat as the integration scheme is adapted to different applications. FIG. 8 shows a step in which an oxide layer 52 is grown over the entire wafer, followed by deposition of a nitride layer 54 and finally a polysilicon layer 56.